Patent

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s): André DeHon, et al.	Re: Information Disclosure Statement
Serial No.: 10/643,772	Group: 2825
Filed: August 18, 2003	Examiner: not yet assigned
For: "ELEMENT PLACEMENT METHOD AND APPARATUS"	Our Ref: B-5138NP 621046-7
	Date: March 19, 2004

Commissioner for Patents
P.O. Box 1450
Alexandria VA, 22313-1450

Sir:

In accordance with the Applicants' duty to disclose information which may be material to the examination of this application, the undersigned respectfully requests that the Examiner consider on the merits the documents listed on the enclosed Form PTO-1449 (modified) before issuing the first Office Action on the merits. Copies of the foreign patent documents and the non-patent publications listed on the enclosed Form PTO-1449 (modified) are enclosed herewith for the Examiner's convenience. Copies of the U.S. patent documents listed on the enclosed Form PTO-1449 (modified) are not enclosed, pursuant to Deputy Commissioner Stephen G. Kunin's Pre OG Notice dated July 11, 2003.

The filing of this Information Disclosure Statement (IDS) shall not be construed as a representation that a search has been made (37 C.F.R. 1.97(g)), an admission that the information cited is, or is considered to be, material to patentability, or that no other material information exists.

The Applicants believe that this IDS is being submitted before the issuance of a first Office Action on the merits and before the issuance of a Final Rejection or Notice of Allowance. Therefore, no official fees should be due; and this IDS should be considered

on the merits. If this IDS is being submitted after the issuance of the first Office Action on the merits and before the issuance of a Final Rejection or Notice of Allowance, please contact the undersigned to authorize a payment of $180.00 (or any other required amount), which is the fee set forth in 37 C.F.R. § 1.97(c), if the Examiner believes that such a fee is due in order for this IDS to be considered on the merits.

The filing of this Information Disclosure Statement shall not be construed as an admission against interest in any manner. (Notice of January 9, 1992, 1135 O.G. 13-25, at 25.)

The person making this statement is the practitioner who signs below on the basis of information supplied by an individual associated with the filing and prosecution of this application (37 C.F.R. § 1.56(c)) and on the basis of information in the practitioner's file.

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first-class mail in an envelope addressed to the "Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450", on March 19, 2004 by Shana Morda.

Respectfully submitted,

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Enclosures: Form PTO-1449 (modified) (3 pages)
Copy of Non-U.S. Patent documents listed on Form PTO-1449 (modified)

Form PTO-1449 (Modified) Page 1 of 3	ATTY DOCKET NO. B-5138NP	U.S. SERIAL NO. 10/643,772
LIST OF PATENTS AND PUBLICATIONS STATEMENT	APPLICANTS André DeHon, et al.	
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U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	ISSUE DATE	NAME	CLASS	SUB-CLASS	FILING DATE or 102(e) DATE IF APPROPRIATE
	5,144,563	9/1992	Date et al.	364	491	
	5,796,625	8/1998	Scepanovic et al.	364	491	

FOREIGN PATENT DOCUMENTS

	DOCUMENT NUMBER	PUBLICATION DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION YES/NO

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

	Alfke, P., "Efficient Shift Registers, LFSR Counters, and Long Psuedo-Random Sequence Generators," *Xilinx Application Note*, XAPP 052, INTERNET: <http://www.xilinx.com/xapp/xapp203.pdf> pp. 1-6 (July 7, 1996).
	Banerjee, P., *Parallel Algorithms for VLSI Computer-Aided Design*, Chapter 3, Englewood Cliffs, New Jersey: PTR Prentice Hall, pp. 118-171 (1994).
	Betz, V., et al., *Architecture and CAD for Deep-Submicron FPGAs*, Boston: Kluwer Acadmeic Publishers, pp. 50-61 (1999).
	Brelet, J., "An Overview of Multiple CAM Designs in Virtex Family Devices," *Xilinx Application Note*, XAPP201, INTERNET: <http://www.xilinx.com/xapp/xapp260.pdf> pp. 1-6 (September 23, 1999).
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	Chan, Pak K., et al., "Parallel Placement for Field-Programmable Gate Arrays," *presented at the Eleventh ACM International Symposium on Field-Programmable Gate Arrays*, Monterey, California, INTERNET: <http://www.doi.acm.org/10.1145/103724.103725> pp. 43-50 (2003).

EXAMINER	DATE CONSIDERED

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

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	Chyan, Dah-Jun, et al., "A Placement Algorithm for Array Processors," *presented at the ACM/IEEE Design Automation Conference*, Miami Beach, Florida, INTERNET: <http://portal.acm.org/citation.cfm?id=800661> pp.182-188 (1983).
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	DeHon, A., et al., "Hardware-Assisted Fast Routing," *IEEE Symposium on Field-Programmable Custom Computing Machines*, Napa Valley, California, INTERNET: <http:www.cs.caltech.edu/research/ic/abstracts/fastroute_feem2002.html> pp. 1-11 (April 22-24, 2002).
	Goto, S., "An Efficient Algorithm for the Two-Dimensional Placement Problem in Electrical Circuit Design," *IEEE Transactions on Circuits and Systems*, Vol. CAS-28, No. 1, pp.12-18 (January 1981).
	Haldar, M., et al., "Parallel Algorithms for FPGA Placement," *Proceedings of the Tenth Great Lakes Symposium on VLSI*, INTERNET: <http://doi.acm.org/10.1145/330855.330988> pp.86-94 (2000).
	Huang, R., et al., "Stochastic, Spatial Routing for Hypergraphs, Trees, and Meshes," *Eleventh ACM International Symposium on Field-Programmable Gate Arrays*, INTERNET:<http://www.cs.caltech.edu/research/ic/abstracts/fastroute_fpga2003.html> 12 pages total (February 23-25, 2003).
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	Mulpuri, C., et al., "Runtime and Quality Tradeoffs in FPGA Placement and Routing," *Proceedings of the Ninth International Symposium on Field-Programmable Gate Arrays*, INTERNET:<http://www.ee.washington.edu/faculty/hauck/publications/RuntimeTradeoffs.pdf> pp. 29-36 (February 11-13, 2001).

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	Sankar, Y., et al., "Trading Quality for Compile Time: Ultra-Fast Placement for FPGAs," *Proceedings of the 1999 ACM/SIGDA Seventh International Symposium on Field Programmable Gate Arrays*, INTERNET:<http://www.eecg.toronto.edu/~jayar/pubs/sankar/fpga99sankar.pdf> pp. 157-166 (1999).
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	Shahookar, K., et al., "VSLI Cell Placement Techniques," *ACM Computing Surveys (CSUR)*, Vol. 23, No. 2, pp.143-220 (June 1991).
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	Tessier, R., "Fast Placement Approaches for FPGAs," *ACM Transactions on Design Automation of Electronic Systems (TODAES)*, Vol. 7, No. 2 pp. 284-305, (April 2002).
	Thompson, C.D., et al., "Sorting on a Mesh-Connected Parallel Computer," *Communications of the ACM*, Vol. 20, No. 4, pp.263-271 (April 1977).

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